CLAIMS

WHAT IS CLAIMED:

1. A memory module, comprising:

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector; and

termination circuitry coupled to at least a subset of the lines.

2. The memory module of claim 1, wherein the termination circuitry further comprises a pull-up resistor coupled to each of the lines in the subset.

3. The memory module of claim 1, further comprising a termination voltage generator adapted to generate a termination voltage signal, the termination circuitry being configured to terminate the subset of the lines using the termination voltage signal.

4. The memory module of claim 3, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage generator.

5. The memory module of claim 3, wherein the termination voltage generator further comprises a voltage regulator.

6. The memory module of claim 3, wherein the termination voltage generator further comprises a voltage divider.

7. The memory module of claim 6, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

8. The memory module of claim 1, wherein the termination circuitry further comprises a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

9. The memory module of claim 1, further comprising a termination voltage line coupled between the connector and the termination circuitry.

10. The memory module of claim 9, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage line.

11. The memory module of claim 1, further comprising enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal.

12. The memory module of claim 11, wherein the enable circuitry further comprises a plurality of switches coupled between the termination circuitry and the lines.

13. The memory module of claim 11, wherein the termination circuitry further comprises switchable resistors configured to receive the termination disable signal.

14. The memory module of claim 11, further comprising a switch configured to provide the termination disable signal.

15. The memory module of claim 11, further comprising a jumper configured to provide the termination disable signal.

16. The memory module of claim 11, further comprising a termination disable signal line coupled to the connector for providing the termination disable signal.

17. The memory module of claim 1, wherein the connector further comprises an edge connector.

18. A memory module, comprising:

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

termination circuitry coupled to at least a subset of the lines;

a termination voltage generator adapted to generate a termination voltage signal and provide the termination voltage signal to the termination circuitry; and

enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal.

19. A system comprising:

a circuit board including a memory bus and an expansion socket coupled to the memory bus; and

a memory module including:

a memory device;

a connector adapted to interface with the expansion socket;

a plurality of lines coupling the memory device and the connector; and

termination circuitry coupled to at least a subset of the lines.

20. The system of claim 19, wherein the termination circuitry further comprises a pull-up resistor coupled to each of the lines in the subset.

21. The system of claim 19, wherein the memory module further comprises a termination voltage generator adapted to generate a termination voltage signal, the termination circuitry being configured to terminate the subset of the lines using the termination voltage signal.

22. The system of claim 21, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage generator.

23. The system of claim 21, wherein the termination voltage generator further comprises a voltage regulator.

24. The system of claim 21, wherein the termination voltage generator further comprises a voltage divider.

25. The system of claim 24, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being

generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

26. The system of claim 19, wherein the termination circuitry further comprises a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

27. The system of claim 19, wherein the memory module further comprises a termination voltage line coupled between the connector and the termination circuitry.

28. The system of claim 27, wherein the termination circuitry further comprises a pull-up resistor coupled between each of the lines in the subset and the termination voltage line.

29. The system of claim 19, wherein the memory module further comprises enable circuitry coupled to the termination circuitry and being configured to disable the termination circuitry responsive to a termination disable signal.

30. The system of claim 29, wherein the enable circuitry further comprises a plurality of switches coupled between the termination circuitry and the lines.

31. The system of claim 29, wherein the termination circuitry further comprises switchable resistors configure to receive the termination disable signal.

32. The system of claim 29, wherein the memory module further comprises a switch configured to provide the termination disable signal.

33. The system of claim 29, wherein the memory module further comprises a jumper configured to provide the termination disable signal.

34. The system of claim 29, wherein the memory module further comprises a termination disable signal line coupled to the connector for providing the termination disable signal.

35. The system of claim 29, wherein the connector further comprises an edge connector.

36. A memory module, comprising:

a memory device;

a connector;

a plurality of lines coupling the memory device and the connector;

a termination voltage line; and

a plurality of pull-up resistors coupled between selected lines of the plurality of lines and the termination voltage line.

37. The memory module of claim 36, further comprising a termination voltage generator coupled to the termination voltage line.

38. The memory module of claim 37, wherein the termination voltage generator further comprises a voltage regulator.

39. The memory module of claim 37, wherein the termination voltage generator further comprises a voltage divider.

40. The memory module of claim 39, wherein the voltage divider further comprises:

a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to the termination voltage line; and

a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground.

41. The memory module of claim 36, further comprising switches coupled between the pull-up resistors and the termination voltage line, the switches being configured to disable the pull-up resistors responsive to a termination disable signal.

42. The memory module of claim 36, wherein the connector further comprises an edge connector.

43. A method for fabricating a memory module, comprising:

providing a circuit board having a connector;

mounting a memory device on the circuit board;

coupling the memory devices to the connector using a plurality of lines;

coupling termination circuitry to at least a subset of the lines.

44. The method of claim 43, wherein coupling the termination circuitry further comprises coupling a pull-up resistor coupled to each of the lines in the subset.

45. The method of claim 43, further comprising:

providing a termination voltage generator on the circuit board; and

coupling the termination voltage generator to the termination circuitry.

46. The method of claim 45, wherein providing the termination circuitry further comprises coupling a pull-up resistor between each of the lines in the subset and the termination voltage generator.

47. The method of claim 45, wherein providing the termination voltage generator further comprises providing a voltage regulator.

48. The method of claim 45, wherein providing the termination voltage generator further comprises providing a voltage divider.

49. The method of claim 48, wherein providing the voltage divider further comprises:

coupling a first terminal of a first resistor to a supply voltage source;

coupling a second terminal of the first resistor to one of the lines in the subset; and

coupling a first terminal of a second resistor to the second terminal of the first resistor; and

coupling a second terminal of the second resistor to ground, the termination voltage signal being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

50. The method of claim 43, wherein providing the termination circuitry further comprises providing a plurality of voltage dividers coupled to the lines in the subset, each voltage divider comprising a first resistor having a first terminal coupled to a supply voltage source and a second terminal coupled to one of the lines in the subset and a second resistor having a first terminal coupled to the second terminal of the first resistor and a second terminal coupled to ground, the termination voltage being generated at the connection of the second terminal of the first resistor and the first terminal of the second resistor.

51. The method of claim 43, further comprising coupling a termination voltage line between the connector and the termination circuitry.

52. The method of claim 51, wherein providing the termination circuitry further comprises coupling a pull-up resistor between each of the lines in the subset and the termination voltage line.

53. The method of claim 43, further comprising coupling enable circuitry to the termination circuitry for disabling the termination circuitry responsive to a termination disable signal.

54. The method of claim 53, wherein providing the enable circuitry further comprises coupling a plurality of switches between the termination circuitry and the lines.

55. The method of claim 53, wherein providing the termination circuitry further comprises providing switchable resistors configured to receive the termination disable signal.

56. The method of claim 53, further comprising providing a switch on the circuit board configured to provide the termination disable signal.

57. The method of claim 53, further comprising providing a jumper on the circuit board configured to provide the termination disable signal.

58. The method of claim 53, further comprising coupling a termination disable signal line to the connector for providing the termination disable signal.

59. A method for terminating a memory bus, comprising:

providing at least two expansion sockets coupled to the memory bus;

interfacing two expansion memory modules including termination circuitry with the expansion sockets; and

disabling the termination circuitry for one of the expansion memory modules.

60. The method of 59, wherein disabling the termination circuitry further comprises setting a switch on one of the expansion memory modules.

61. The method of 59, wherein disabling the termination circuitry further comprises providing a termination disable signal to one of the expansion memory modules.